REMARKS

Claims 11-34 will be pending upon entry of the present amendment. Claims 1-10 are being canceled. Claims 13-14 are being amended. Claims 23-34 are new. No new matter is being submitted.

Claim 13 is being amended to correct a typographical error. Claim 14 is being amended to remove language that was misdescriptive.

The applicants appreciate the indication that claims 13-17 are directed to allowable subject matter. Claims 13-17 are not being placed in independent form because the applicant submits that claim 11, from which claims 13-17 depend, is in condition for allowance as explained below.

Claims 11-12 and 18-22 were rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent Application Publication No. 2003/0028756 to Panis et al. ("Panis").

The Examiner has not established a *prima facie* case of obviousness. In particular, the Examiner has not satisfied any of the criteria set forth in MPEP § 706.02(j) for establishing a *prima facie* case of obviousness. MPEP § 706.02(j) states:

> to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck,* 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

The Examiner does not provide any suggestion or motivations for modifying Panis to obtain the claimed invention, or provide any reasonable expectation of success.

In addition, Panis does not teach or suggest all of the claim limitations recited in claim 11. In fact, the applicant submits that Panis does not teach or suggest any of the claim limitations recited in claim 11. First, Panis does not teach or suggest a device for transferring data between asynchronous first and second systems. Panis does not mention or suggest any

asynchronicity. The Examiner points to a first command execution unit BAU1 as being the first system and the command execution units BAU2-BAU4 as being a second system, but nothing in Panis suggests that those systems operated asynchronously.

Second, Panis does not teach or suggest write and read pointer registers in first and second systems, respectively. The Examiner points to paragraph 0107 as showing such registers, but paragraph 0107 specifically states that write and read pointers are stored in the same stack SS. Thus, such write and read pointers cannot be write and read pointer registers in first and second systems, respectively. Panis nowhere suggests that such write and read pointers could or should be stored respectively in write and read pointer registers of first and second systems, respectively.

Third, Panis does not teach or suggest a buffer memory connected between asynchronous first and second systems. As discussed above, Panis does not teach or suggest asynchronous first and second systems, and thus, cannot suggest a buffer memory connect between such systems.

Fourth, Panis does not teach or suggest first, second, and third shadow registers located and connected as recited in claim 11. In particular, Panis does not teach or suggest first and second shadow registers connected to receive the contents of the write and read pointer registers, respectively. Panis shows shadow registers SR1-SR4 in the prior art device of Figure 6 while the write and read pointers are part of the stack SS of the device of Figure 1 that is intended to overcome the problems associated with the shadow registers of Figure 6. Thus, Panis teaches away from combining the shadow registers SR1-SR4 with the write and read pointers. In addition, Panis does not teach or suggest a third shadow register connected to receive the contents of the second shadow register. Instead, Panis states that the shadow registers are respectively associated with the command execution units BAU1-BAU4 (para. 0104), and thus, the contents of any one of the shadow registers SR1-SR4 will never be transferred to any of the other shadow registers.

Fifth, Panis does not teach or suggest a first compare circuit that compares the contents of the write pointer register with the contents of the third shadow registers. As discussed above, the write pointer and shadow registers SR1-SR4 are part of separate devices of

Figs. 1 and 6, and Panis teaches away from combining the two devices. In addition, Panis never mentions or suggest any compare device that compares the contents of any registers.

For at least the foregoing reasons, claim 11 is nonobvious in view of Panis.

Claims 12 and 18-19 depend on claim 11, and thus, are nonobvious for the reasons expressed above. In addition, Panis does not teach or suggest any of the elements recited in claims 12 and 18-19. That is, Panis does not teach or suggest a handshake circuit, a dual port FIFO memory, or asynchronous first and second systems integrated in the same semiconductor product.

Although the language of claims 20-22 is not identical to that of claim 11, the allowability of claims 20-22 will be apparent in view of the above remarks.

Claims 11-12 and 18-22 were rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent Application Publication No. 2003/0023836) to Catherwood et al. ("Catherwood").

As with Panis, the Examiner has not established a *prima facie* case of obviousness with respect to Catherwood. In particular, the Examiner has not satisfied any of the criteria set forth in MPEP § 706.02(j) for establishing a *prima facie* case of obviousness. The Examiner does not provide any suggestion or motivations for modifying Catherwood to obtain the claimed invention, or provide any reasonable expectation of success.

In addition, Catherwood does not teach or suggest all of the claim limitations recited in claim 11. In fact, like Panis, the applicant submits that Catherwood does not teach or suggest any of the claim limitations recited in claim 11. First, Catherwood does not teach or suggest a device for transferring data between asynchronous first and second systems. Catherwood does not mention or suggest any asynchronicity. The Examiner points to a processor 100 as being the first system and external devices 140 as being a second system, but nothing in Catherwood suggests that those systems operated asynchronously.

Second, Catherwood does not teach or suggest write and read pointer registers in first and second systems, respectively. The Examiner points to paragraph 0043 as showing such registers, but paragraph 0043 mentions only a single instruction pointer. Thus, such a single instruction pointer cannot be both write and read pointers, is not stored in write and read

registers, and does not suggest write and read registers in asynchronous first and second systems, respectively. In addition, Catherwood does not suggest the instruction pointer is stored in the external devices 140 that the Examiner indicated to be the second system.

Third, Catherwood does not teach or suggest a buffer memory connected between asynchronous first and second systems. As discussed above, Catherwood does not teach or suggest asynchronous first and second systems, and thus, cannot suggest a buffer memory connect between such systems.

Fourth, Catherwood does not teach or suggest first, second, and third shadow registers located and connected as recited in claim 11. In particular, Catherwood does not teach or suggest first and second shadow registers connected to receive the contents of the write and read pointer registers, respectively. Catherwood shows shadow registers 350, but nothing in Catherwood suggests that any of the registers 350 receive the contents of write and read pointer registers. Instead, Catherwood states that the shadow registers 350 may temporarily store data values of various primary registers that include working registers, program counter register, repeat loop counter register, a do loop count register, and a status register (0044-0045) without ever mentioning any write or read pointer registers. In addition, Catherwood does not teach or suggest a third shadow register connected to receive the contents of the second shadow register. Instead, Catherwood states that the shadow registers are respectively associated with the primary registers, and not with each other.

Fifth, Catherwood does not teach or suggest a first compare circuit that compares the contents of the write pointer register with the contents of the third shadow registers. As discussed above, the Catherwood does not suggest any write pointer register. In addition, Catherwood never mentions or suggest any compare device that compares the contents of any registers.

For at least the foregoing reasons, claim 11 is nonobvious in view of Catherwood.

Claims 12 and 18-19 depend on claim 11, and thus, are nonobvious for the reasons expressed above. In addition, Catherwood does not teach or suggest any of the elements recited in claims 12 and 18-19. That is, Catherwood does not teach or suggest a handshake

circuit, a dual port FIFO memory, or asynchronous first and second systems integrated in the same semiconductor product.

Although the language of claims 20-22 is not identical to that of claim 11, the allowability of claims 20-22 will be apparent in view of the above remarks.

If the Examiner continues to assert either of Panis and Catherwood against the claims, the applicant respectfully requests that the Examiner point to specific teachings of asynchronous systems, the connections of the elements in claim 11, the handshake circuit of claim 12, the dual port FIFO memory of claim 18, and the integrated device of claim 19.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

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